AN ENHANCED POWER DC-AC BUCK CONVERTER

CONVERTIDOR BUCK CC-CA DE POTENCIA MEJORADA

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ABSTRACT:

This paper presents an enhanced power DC-AC buck converter. The main aim of this research paper is to ensure that the conventional H-bridge DC-AC buck converter is operated practically without delay time between the complementary power switches on the same leg. The enhanced version is realized by serially connecting sized inductor-capacitor-diode topology between the drains and the sources of the high sides of the H-bridge converters. The significant improvement in this kind of converter is that it offers short-circuit immune systems that are not obtainable in the traditional buck DC-AC converter and it triggers the complementary power switches without delay time. The power circuit is obtained by an amalgamation of two Y-closed-up topologies to form an H-bridge converter. The proposed system has a power rating of 3.25 kW, THD of 0.2717%, and pure sine waveforms of output voltage and current of 311.00V and 10.63A under resistive loads. Under RL loads, it offers 3.25 kW, THD of 0.2807%, and pure sine waveforms of output voltage and current of 297.5V and 10.925A

Keywords: DC-AC Converter, traditional, Buck, Enhanced, Power

RESUMEN:

Este trabajo presenta un convertidor buck DC-AC de potencia mejorada. El objetivo principal de este trabajo de investigación es conseguir que el convertidor buck CC-CA de puente en H convencional, funcione prácticamente sin tiempo de retardo entre los interruptores de potencia complementarios de la misma pata. La versión mejorada se realiza conectando en serie la topología inductor-condensador-diodos dimensionados entre los drenajes y las fuentes de los lados altos de los convertidores puente H. La mejora significativa de este tipo de convertidor es que ofrece sistemas inmunes al cortocircuito que no se pueden obtener en el convertidor DC-AC buck tradicional y activa los interruptores de potencia complementarios sin tiempo de retardo. El circuito de potencia se obtiene mediante una amalgama de dos topologías de cierre en Y para formar un convertidor de puente en H. El sistema propuesto tiene una potencia nominal de 3,25 kW, una THD del 0,2717% y formas de onda sinusoidales puras de tensión y corriente de salida de 311,00V y 10,63A bajo cargas resistivas. Bajo cargas RL, ofrece 3,25 kW, THD del 0,2807%, y formas de onda sinusoidales puras de tensión y corriente de salida de 297,5V y 10,925A.

Palabras clave: Convertidor DC-AC, tradicional, Buck, Mejorado, Potencia.

1. - INTRODUCTION

A Power DC-AC converter is a system that acts on DC power to realize an AC power at a preferred frequency and power per current. The conversion is done by firing its power electronics switches with appropriate switching pulses from a control unit. The DC power sources that are acted upon by the DC-AC converter can be obtained from solar panels, rectified/filtered AC power supply, super capacitors, fuel cells, etc. The switching pulses are derived from varieties of modulation schemes like sinusoidal pulse-width modulations, space vector pulse-width modulation, in-phase disposition-based pulse-width modulation technique, phase opposition disposition PWM, alternate phase disposition PWM, phase shift PWM, improved space vector modulation schemes, enhanced selective harmonic elimination scheme, etc. [1]- [3].

Globally, there are many areas of applications for DC-AC power converters such as grid-connected power inverters, lighting our homes and industries, industrial motor drives, powering hospital equipment, and telecommunication centers [4-5].

The Power inverter (Power DC-AC converter) can be divided into various categories, such as, current and voltage DC-AC converters, single phase and three phase inverters, transformer and non-transformer dependent inverters, multilevel and multiphase inverters and so on with different performance characteristics.

Even though the conventional single-phase buck inverter displayed in Fig.1 has lower component count and is easy to develop, it has high total harmonic distortions. It also damages instantly whenever the two complementary power switches on the same leg are triggered practically, using complementary pulses, without gapping or delay times. Other derivatives of conventional H-bridge inverters such as those in [6-8] are also included in working under delay time-based switching signals between the complementary power switches on the same leg of inverters.

The main aim of this research paper is to practically solve the problems of switching complementary power switches on the same leg of conventional single-phase full bridge inverters under complementary pulses without gapping or delay times using two Y-closed -up configurations of active and passive components.

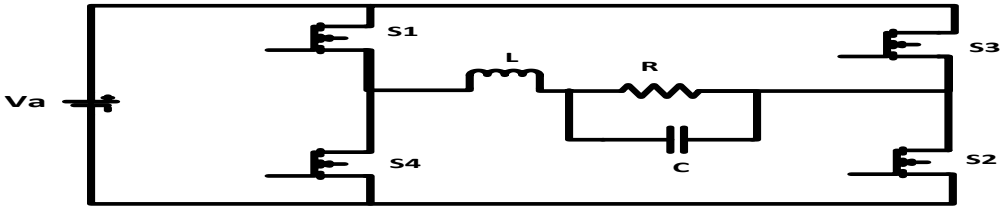

Fig.1. Conventional single-phase buck DC-AC converter, source [9]-[12]

2. -METHODOLOGY

Analytical/simulation and implementation methods are adopted in this research work. The proposed circuit diagram is shown in Fig.2. The power circuit of the converter system is formed by two Y-closed -up configurations. The Y-closed-up topologies with their components are connected parallel to each other to produce an H-bridge structure. Then, they are connected to the load through an inductance-capacitance filter (L3 and C3). They can also be connected to the load without the filter components depending on their applications.

To produce an AC power, the S1 and S2 are turned ON while S3 and S4 are turned OFF at the same time during the positive half-cycle. But during the negative half cycle, S3 and S4 are switched ON while S1 and S2 are turned OFF at the same moment like the conventional DC-AC power converter. Unlike the conventional DC-AC power converter that blows out or burns its power switches due to short-circuit conditions when S1 and S2 are turned ON practically without being well-gapped, the proposed circuit diagram keeps the two switches on the same leg safe. In this circuit, the current flows through $S_1 \rightarrow L_1 \rightarrow L_3 \rightarrow Z_L \rightarrow C_2 \rightarrow D_2 \rightarrow S_1$ to charge the capacitor before it discharges to the load during the positive half-cycle. If the short-circuit situation appears during the negative half cycles as a result of S3 and S4 being switched on at the same time, the condition is arrested by the current passing through the loop $S_1 \rightarrow L_1 \rightarrow C_1 \rightarrow D_1$ and subsequently discharges to load.

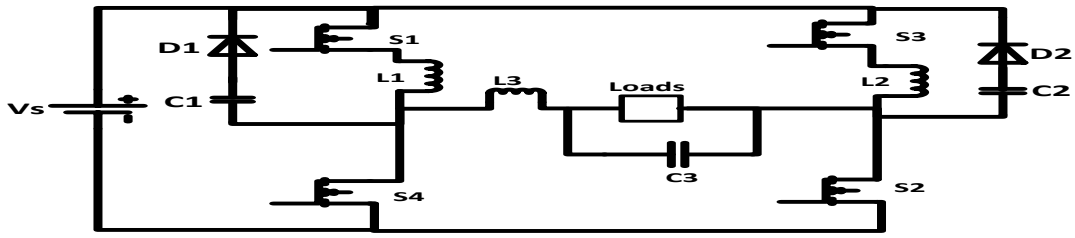

Fig.2.The proposed circuit diagram

3. -STABILITY ANALYSIS OF THE PROPOSED CIRCUIT

Naturally, in linking up a DC-AC converter system to loads such as resistive loads, inductive loads, resistive-inductive loads, grid network, etc., at any moment, there is always the occurrence of instability at their point of intersection [13]. In this research work, a small-signal model is adopted to analyze the proposed system using a square voltage per power approach (SVPPA) [14]. SVPPA is an impedance-based scheme. It is dependent on the Nyquist criterion and eigenvalue of the inverter output admittance and the load impedance matrices in the frequency domain for analyzing the stability of the inverter-load system. So, for critical analysis of the

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proposed system, the inverter side is first modeled as a Thevenin source and then, it is connected to the load part. In order to model the inverter side first, the load system is removed. The Thevenin impedance circuit configuration for the determination of the inverter is shown in Fig.3

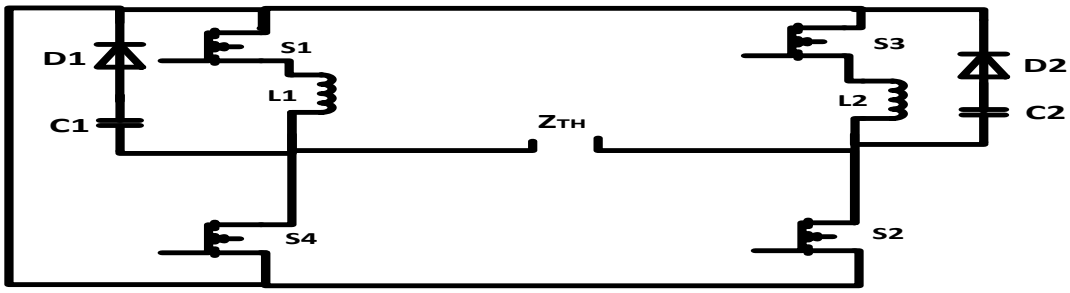

Fig.3.Thevenin Impedance circuit of the proposed system.

The expression of the Thevenin impedance of the circuit in Fig.3 is deduced as in eq. 1

$$Z_{TH} = \left(\left[\left(Z_{D1} + Z_{C1}\right)//\left(Z_{S1} + Z_{L1}\right)\right]//\left[Z_{S4}\right]\right) + \left[\left(Z_{D2} + Z_{C2}\right)//\left(Z_{S3} + Z_{L2}\right)\right]//\left[Z_{S2}\right] \quad (1)$$

The Thevenin voltage of Fig.4 is expressed in eq.2

$$V_{TH} = i_1\left(Z_{S1} + Z_{L1}\right) + i_2\left(Z_{S3} + Z_{L2}\right) \quad (2)$$

Where Z_{D1}, Z_{C1} , Z_{S1}, Z_{L1}, Z_{S4} , Z_{D2} , Z_{C2}, Z_{S3}, Z_{L2} and Z_{S2} are the impedances of power diode D1, capacitor 1, power MOSFET S1, inductor L1, power MOSFET S4, power diode,D2, the capacitance of the capacitor, C2, power MOSFET, S3, inductance of inductor, L2, and power MOSFET S4 respectively.

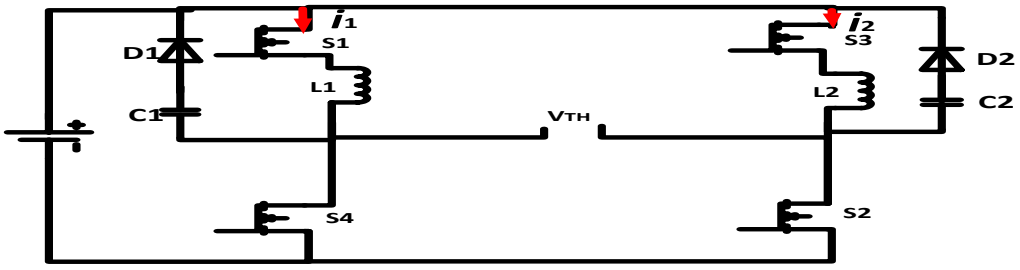

Fig.4. Thevenin voltage circuit of the proposed system

The eqs. 1 and 2 are then coupled back to the load as shown in Fig.5a to represent the Thevenin analytical model of the proposed system.

The load current is represented as in eq.3

$$I_L(s) = \frac{V_{TH}(s)}{Z_{TH}(s) + Z_L(s)} \quad (3)$$

The modeled inverter Thevenin voltage source in Fig.5a is transformed into Norton's current source using eq.3 to deduce eq.4.

$$I_N(s) = \frac{V_{TH}(s)}{Z_T(s)} = V_{TH}(s)Y_N(s) \quad (4)$$

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Where $Y_N(s)$ is the total admittance of the proposed inverter

The transformed inverter current source is coupled back to the load system as shown in Fig.5b for the proposed circuit stability analysis.

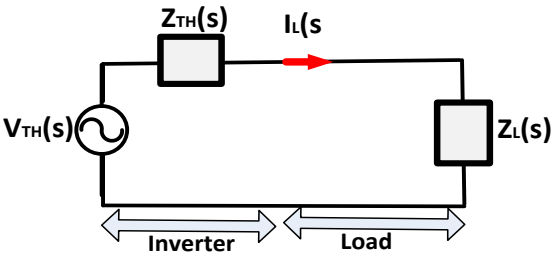

Fig.5a Thevenin analytic model of the proposed system

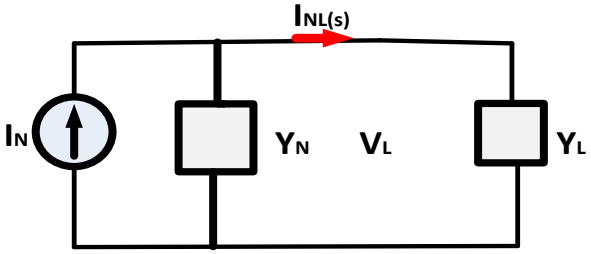

Fig.5b Small-signal equivalent circuit of the proposed system

Then, considering, Fig.5b, the current that is supplied to the load is expressed as

$$I_{NL}(s)=\frac{I_N(s)}{1+Y_N(s)Z_L(s)}-\frac{Y_N(s)V_L(s)}{1+Y_N(s)Z_L(s)} \tag{5}$$

So, applying Nyquist's criterion at the denominator of eq.5, the proposed system is said to be stable if the phase disparity between $Y_N(s)$ and $Z_L(s)$is within an angle interval of 180º i.e. the absolute value of$1+Y_N(s)Z_L(s)$ is less than 1 at operating frequency with difference at 180º.

4. – PERFORMANCE ANALYTIC CHARACTERISTICS OF VOLTAGES ACROSS C1-D1 AND C2-D2

The C1-D1 and C2-D2 attachments are the routes that ensure short-proof current flow during the transfer of switching transitions from positive half-cycle to negative half–cycles without delay times. During the positive half-cycle, as in Fig.6, S1 and S2 are closed with zero (negligible) impedances while S3 and S4 are opened with infinite impedances; the loop currents I_1 and I_2 flow through $V_S \rightarrow S_1 \rightarrow L_1 \rightarrow L_3 \rightarrow Z_L \rightarrow S_2 \rightarrow V_S$ and $S_1 \rightarrow L_1 \rightarrow L_3 \rightarrow Z_L \rightarrow C_2 \rightarrow D_2 \rightarrow S_1$ respectively. The voltage equation that describes the condition is expressed in eq.6

$$\begin{bmatrix} -V_S \\ 0 \end{bmatrix}=\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}\begin{bmatrix} Z_{L1}+Z_L & -Z_{L1}-Z_{L2} \\ -Z_{L1}-Z_{L2} & Z_{L2}+Z_L+Z_{D2}+Z_{C2} \end{bmatrix} \tag{6}$$

The flowing branch current I_{C2-D2}, which is equal to the loop current vía C2-D2 path is deduced from eq.6 and expressed as in eq.7

$$I_1=I_{C2-D2}=\frac{-V_S\left(+Z_{L2}+Z_L+Z_{D2}+Z_{C2}\right)}{\left(Z_{L1}+Z_L\right)\left(Z_{L2}+Z_L+Z_{D2}+Z_{C2}\right)-\left(-Z_{L1}-Z_{L2}\right)^2} \tag{7}$$

The operating voltage V_{C2-D2}, across the C2- D2 is written as

$$V_{C2-D2}=\frac{-V_S\left(Z_{L2}+Z_L+Z_{D2}+Z_{C2}\right)}{\left(Z_{L1}+Z_L\right)\left(Z_{L2}+Z_L+Z_{D2}+Z_{C2}\right)-\left(-Z_{L1}-Z_{L2}\right)^2}\left(Z_{D2}+Z_{C2}\right) \tag{8}$$

During the negative half-cycle, according to Fig.7, S3 and S4 are turned ON with negligible impedances; the loop currents, I_3 and I_4 pass via $V_S \rightarrow S_4 \rightarrow C_1 \rightarrow D_1 \rightarrow V_S$ and

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$S_3 \rightarrow L_2 \rightarrow Z_L \rightarrow L_3 \rightarrow C_1 \rightarrow D_1 \rightarrow S_3$ respectively. The voltage equation that describes the situation is expressed in eq. 9

$$\begin{bmatrix} V_S \\ 0 \end{bmatrix} = \begin{bmatrix} I_3 \\ I_4 \end{bmatrix} \begin{bmatrix} Z_{C1} + Z_{D1} & -Z_{D1} - Z_{C1} \\ -Z_{D1} - Z_{C1} & Z_{D1} + Z_{C1} + Z_{L3} + Z_L + Z_{L2} \end{bmatrix} \quad (9)$$

The current flowing through the C1-D1 path, and the voltage, V_{C1-D1}, across them are written in eq. 10 and 11

$$I_{C1-D1} = I_3 - I_4 = \frac{\left[V_S\left(Z_{D1} + Z_{C1} + Z_{L3} + Z_L + Z_{L2}\right)\right] - \left[-V_S\left(-Z_{D1} - Z_{C1}\right)\right]}{\left(Z_{C1} + Z_{D1}\right)\left(Z_{D1} + Z_{C1} + Z_L + Z_{L3} + Z_{L2}\right) - \left(-Z_{D1} - Z_{C1}\right)^2} \quad (10)$$

$$V_{C1-D1} = \frac{\left[V_S\left(Z_{D1} + Z_{C1} + Z_{L3} + Z_L + Z_{L2}\right)\right] - \left[-V_S\left(-Z_{D1} - Z_{C1}\right)\right]}{\left(Z_{C1} + Z_{D1}\right)\left(Z_{D1} + Z_{C1} + Z_L + Z_{L3} + Z_{L2}\right) - \left(-Z_{D1} - Z_{C1}\right)^2}\left[Z_{D1} - Z_{C1}\right] \quad (11)$$

The eqs. 11 and 8 have the same magnitudes but are phase-shifted at 180º from each other.

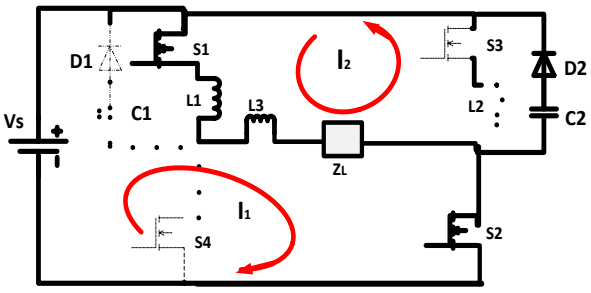

Fig.6. Circuit topology for positive-half cycle

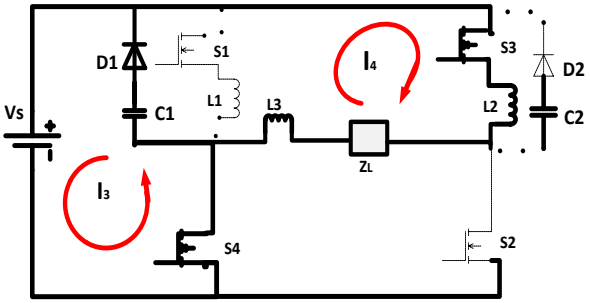

Fig.7. Circuit topology for negative-half cycle

5. – MODULATION SCHEME

The proposed system power switches are controlled using the unipolar-based sinusoidal pulse-width modulation (UBSPWM) technique [15]. It is realized by comparing sine reference signals and carrier waves. UBSPWM is obtained in eqs. 12-17

$$u_{ref1} = v_m sin\theta_i \quad (12)$$

$$u_{ref2} = v_m sin(\theta_i - 180) \quad (13)$$

$$C_W = \begin{bmatrix} 0 & \frac{1}{4f_c} & \frac{1}{2f_c} & \frac{3}{4f_c} & \frac{1}{f_c} \\ 0 & A_t & 0 & A_t & 0 \end{bmatrix} \quad (14)$$

The eq.s 12, 13, and16 are used to produce the modulating signal at 0º,u_{ref1}, modulating signal operating at 180º, u_{ref2} and a carrier wave(C_W). By comparing eqs.12 and 13 with eq.14, and complementing the outputs of their comparisons, eq.s 15-18 are obtained.

$$S_1 = \begin{cases} 1 & if\ u_{ref1} > C_w \\ 0 & ,else \end{cases} \quad (15)$$

$$S_4 = \overline{S_1} \quad (16)$$

$$S_3 = \begin{cases} 1 & if\ u_{ref2} > C_w \\ 0 & ,else \end{cases} \quad (17)$$

$$S_2 = \overline{S_3} \quad (18)$$

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Fig.8 represents a Simulink model of the conventional inverter with total harmonic distortions (THD) of 5.714%, whereas Fig.9 illustrated the Simulink model of the proposed DC-AC power converter with total harmonic distortions (THD) of 0.2717% under resistive load.

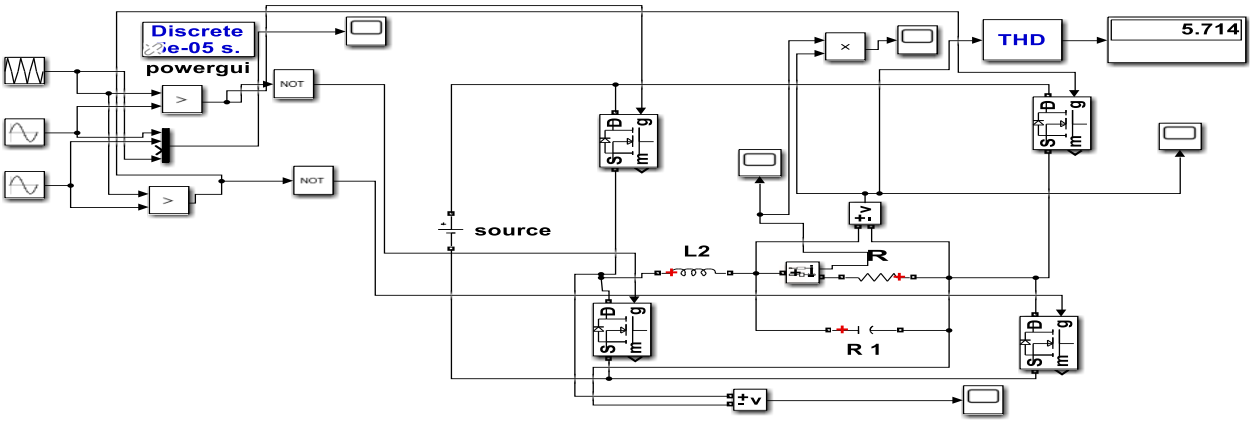

Fig. 8. Simulink model of Conventional Buck DC-AC Converter system in MatLab/ Simulink 2018a under resistive load

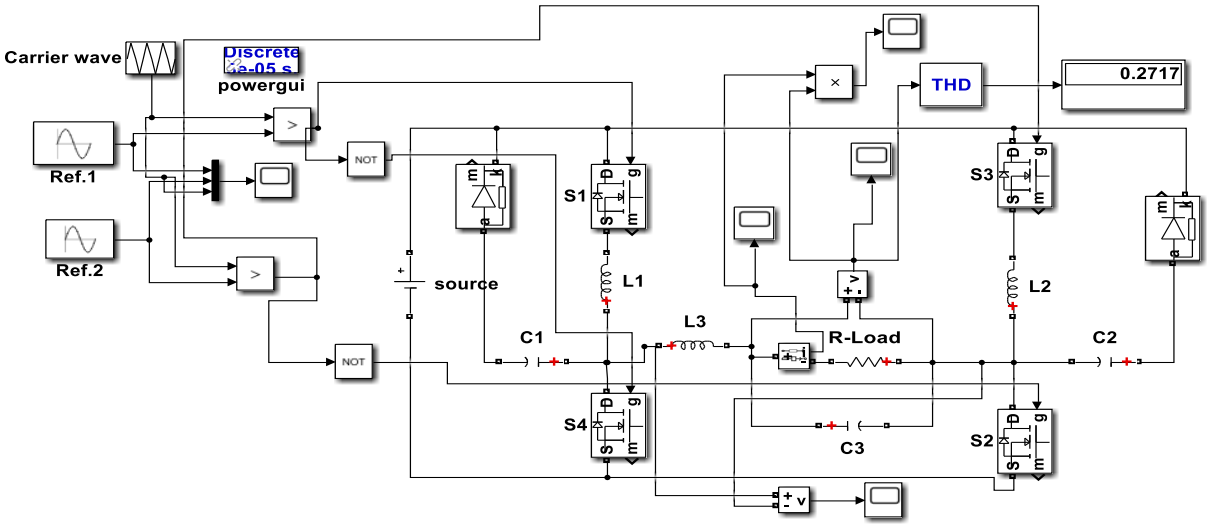

Fig. 9. Simulink model of proposed Power buck inverter modeled in MatLab/ Simulink 2018a under Resistive Load

The Simulink model of the proposed system under resistive-inductive (R-L) loads is shown in Fig. 10. It has a similar topology to the one in Fig.9 except that it has an R-L load and its percentage of total harmonic distortions is 0.2807%.

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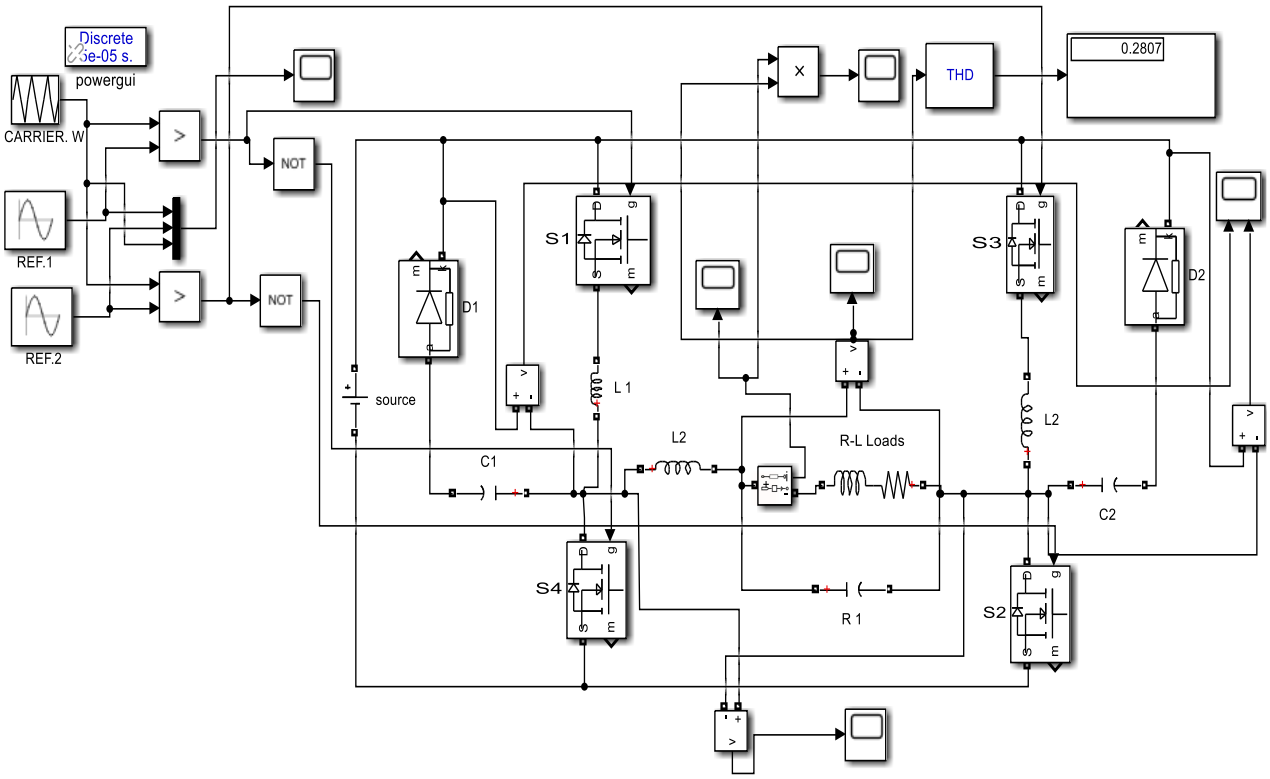

Fig.10. Simulink model of proposed Power buck inverter modeled in MatLab/ Simulink 2018a under R-L Load

6. - DISCUSSION OF SIMULATION RESULTS

The performance characteristics of the simulated proposed system (PS) are shown in Fig.11-15. Fig.11 shows that S1 and S2 are complementary switching pulses with a maximum voltage of 1.0V while S3 and S4 are also complementary switching pulses with the same voltage amplitudes whose mathematical expressions have already been represented in eqs.15-18.

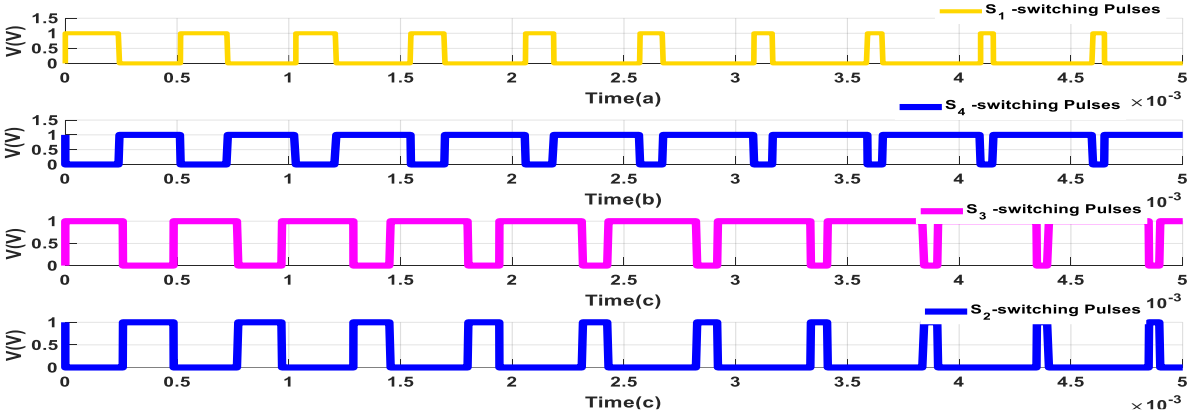

Fig.11(a-c). Switching pulses of the proposed system.

The voltage profiles across C1-D1 and C2-D2 of the PS represented in eq.s 11 and 8 displayed are in Fig. 12a and Fig.12b. It is noticed that they have the same amplitudes of 300V but are phase-shifted at 180 degrees.

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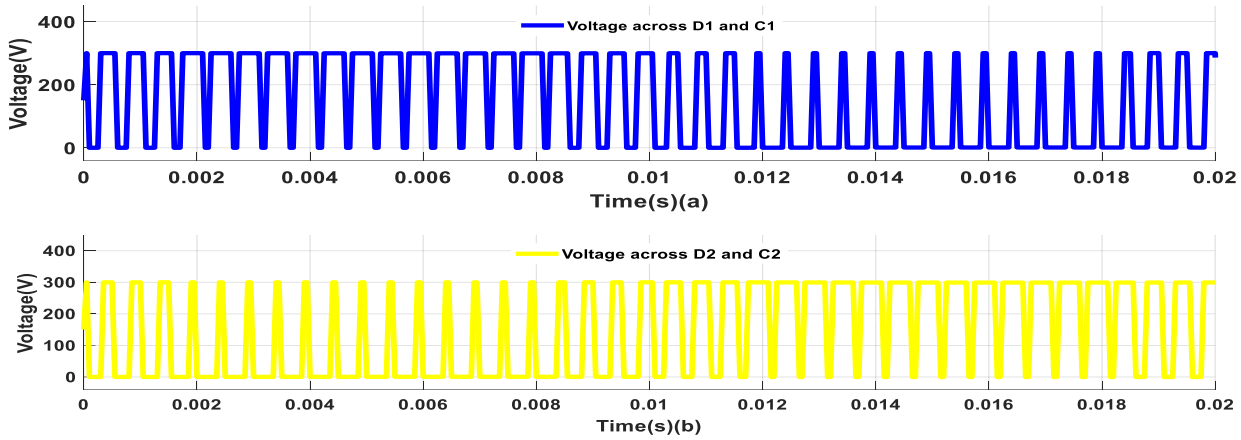

Fig.12a: Voltage across C1-D1 of the proposed system. Fig.12b: Voltage across C2-D2 of the proposed system

The 307.9V unfiltered voltage, a pure sine wave of 305.7V filtered voltage, and 10.63A current of the proposed system are represented in Fig13a, and Fig.13b respectively under resistive load.

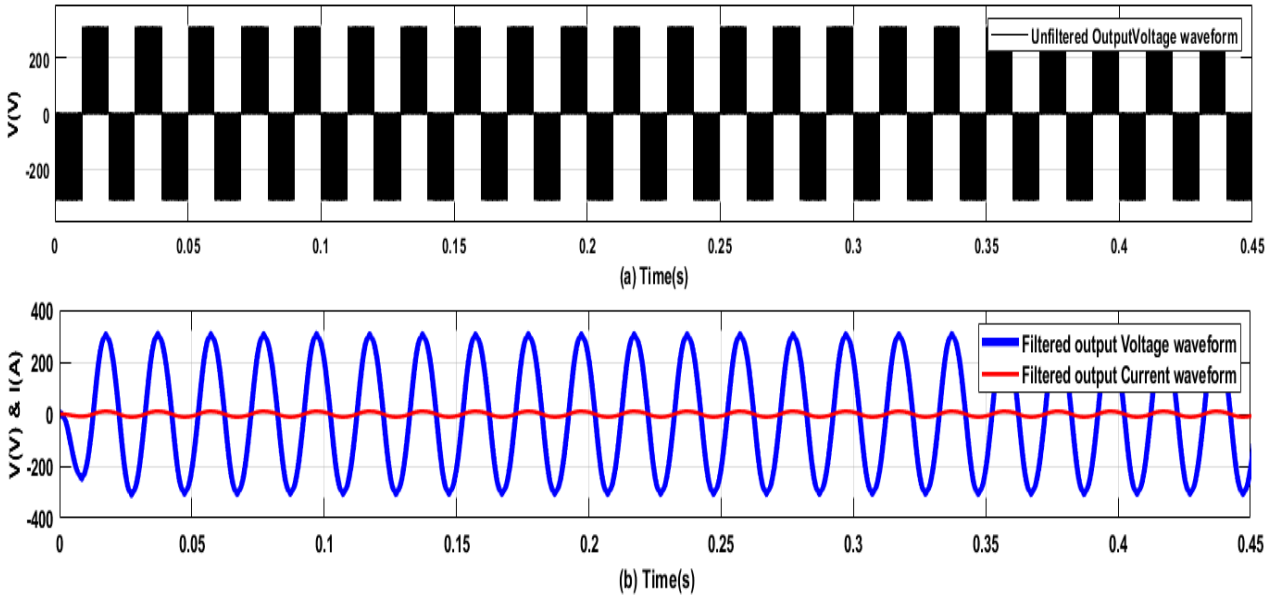

Fig.13 (a). Unfiltered output voltage. Fig.13 (b). Filtered output voltage and current under resistive load

The spectral characteristics of the output voltage are portrayed in Fig.14. In addition, it is observed that at an operating frequency of 50Hz, the total harmonic distortions (THD) and maximum output voltage were 0.2717% and 305.7V. The THD shown in Fig.14 corresponds to the value displayed in Fig.9

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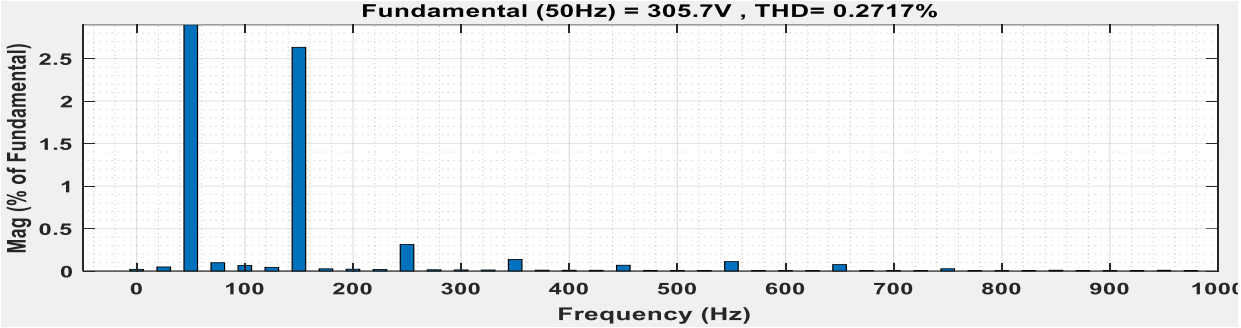

Fig. 14. Spectral display of output filtered voltage of the proposed system

The pure sinewave waveforms of the output voltage and current of 297.4|V and10.92A under the R-L loads are portrayed in Fig.15a respectively. It is observed that the transient response of the proposed system existed at the time interval of $0 \leq t \leq 0.125$second and stabilized at $0.125 \leq t \leq 0.5$second. Fig.15b illustrates the spectral harmonic analyses of output under the R-L loads. In addition, it demonstrates that at 50Hz, the output voltage of 297.4V has a THD of 0.2807%.

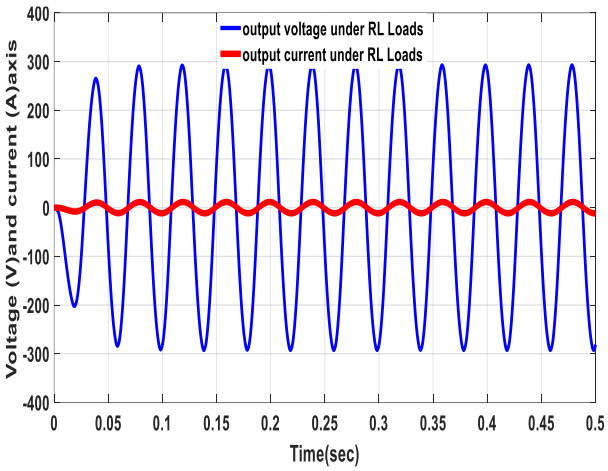

Fig.15. a filtered output voltage and current

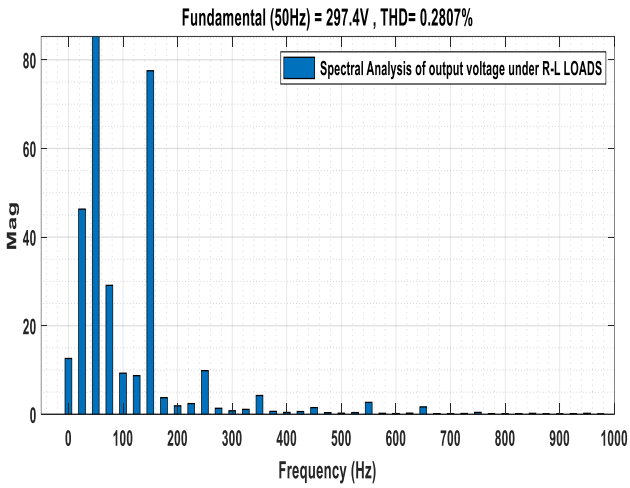

Fig. 15b. Spectral display of output filtered voltage of the proposed the system under RL loads

7. - EXPERIMENTAL RESULTS AND DISCUSSIONS

The experimental results of the proposed system are shown in Fig. 16-19. Fig. 16a illustrates an oscilloscopic display of switching pulses for S1 and S4 used in turning ON/OFF of S1 and S4 power switches. It is noticed that the two switching pulses have no delay times. S1 and S4 pulses have amplitudes of 15.6V and 11.4 Vat an operating frequency of 1.56 kHz. S2 and S3 pulse trains are shown in Fig.16b with peak voltages of 15.2V and 14.4V at 1.55 kHz. It is also observed that S2 and S3 pulses have no delay time between the complementary switching signals. The wave shapes of the pulse trains indicated that the upper switching pulses are stressed more than the lower switching pulses due to their uneven rectangular wave shapes. The simulated results of Fig.16a and Fig.16b have been shown in Fig.11.(a-c) and mathematically written in eq.s15-18.

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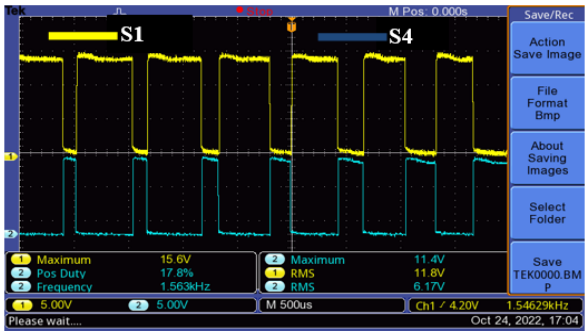

Fig.16(a).S1 and S4 triggering Pulses, (RIGHT)

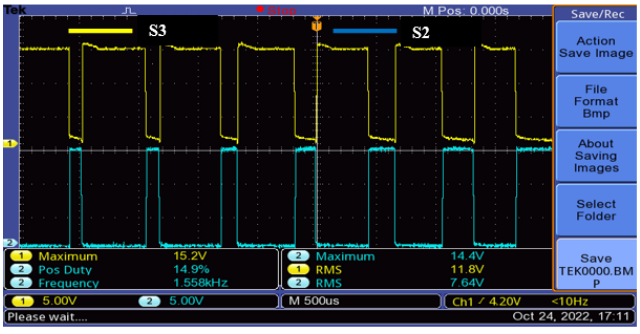

Fig.16(b). S1 and S2 triggering Pulses, (LEFT)

The output voltage profile of the proposed system before the LC filter is displayed in Fig.17a and it has a maximum voltage of 250V. It is a practical demonstration of the wave shape already shown in Fig. 13a. At this level, the output voltage distortion is still high.

The practical demonstrations of voltages across C2-D2 and C1-D1 of eq.8 and eq.11 as well as simulated in Fig12a and Fig.12b are presented in Fig.17b.They have voltage values of 264V and 256V. But due to how they appeared very large on the digital oscilloscope, probes that divided the amplitudes by 10 were used to obtain their waveforms. Their experimented amplitudes differed by 0.8V or (0.8 x10).

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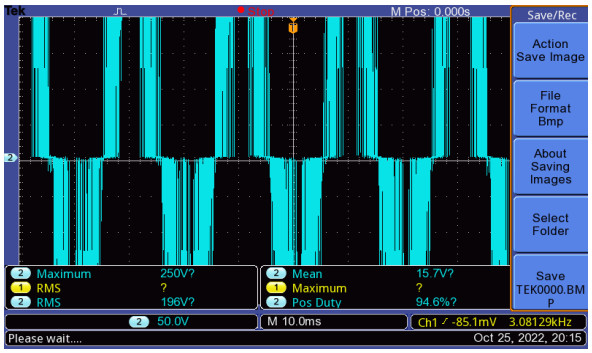

Fig.17a. Experimented unfiltered output voltage of PS

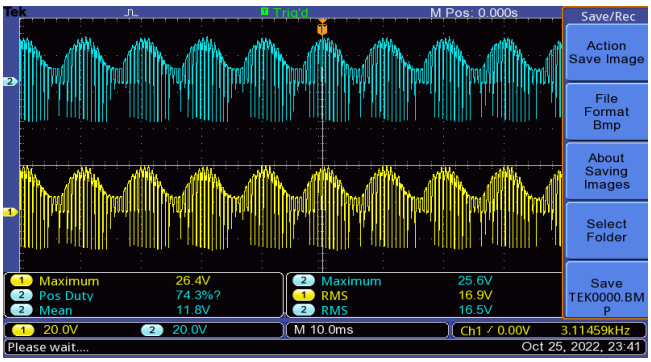

Fig.17b Voltages across the C1-D1 and C2-D2 Components

The 272VDC voltage supply that is manipulated by the enhanced DC-AC buck inverter of the proposed system is shown in Fig.18a. This Fig.18a is inverted and filtered to realize the inverter output waveform displayed in Fig.18b. The filtered output voltage waveform of the proposed system is illustrated in Fig.18b. It showed a voltage of pure sinewaveof260V peak at 49.54 Hz.

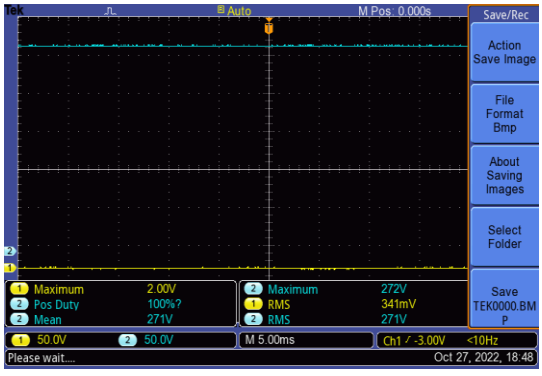

Fig.18a. DC voltage supply

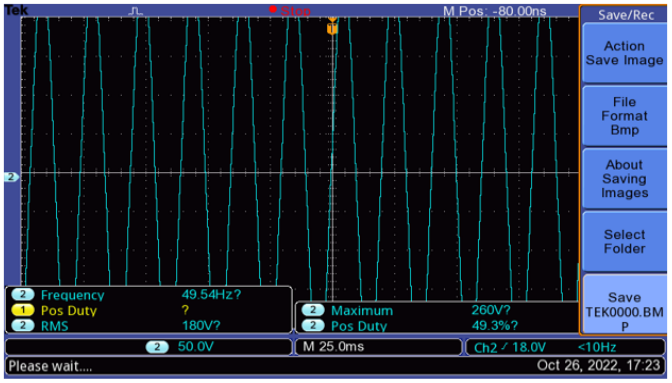

Fig.18b. Filtered output voltage of the proposed system under RL

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The un-energized prototype of the proposed system is shown in Fig.19a while in Fig.19b portrays active working operation of the prototype of the proposed system under R-L loads

Fig.19a. Un-energized prototype of the proposed system.

Fig.19b. An energized prototype of the proposed system

Table.1 represents the items of the simulated and experimental results and components used in this research work.

Items	***Simulated results of Proposed DC-AC Power converter under RL loads***	***Experimental results of Proposed DC-AC Power converter under RL loads***
Input DC voltage supplied	*311.0VDC*	*270VDC*
L1, L2	*1.0μH, 1.0μH*	*(1.0μH -5 μH), (1.0μH -5μH),*
C1,C2	*2.0μF , 2.0μF*	*2.0μF-50μF- at 450V, 2.0μF-50μF- at 450V,*
Voltages across C1-D1 and C2-D2	300V and 300V	264V and 256V
Switching voltage of S1-S4	*1.0V*	*11.4V-15.6V*
Load resistance and inductance	*28.0Ω, 20mH*	*28.0 Ω ,minimum of 20mH*
AC Output voltage	*305.7V*	*260Vpeak*
Input /out voltage ratio	*1.02*	*1.03*
Modulating frequency	*50Hz*	*50Hz*
Switching frequency	*1.5kHz*	*1.563 - 1. 58kHz*
Load Current	*10.92A*	*11.2A*
Power output	*3250W*	*2912W*
Nature of the voltage Waveform	*Pure sinewave*	*Pure sinewave*

Table 1.Tabulated items of the simulated and experimental results and components

8. -CONCLUSION

An enhanced power DC –AC buck power converter has been presented, analyzed, and simulated in MatLab/Simulink 2018a environment and the experiment was carried out at Laboratory of Industrial Electronics, Power Devices, and New Energy Systems University of Nigeria, Nsukka. The results indicated that the proposed system is highly stable and reliable with a short-circuited immune system under the complementary power switches without delay times between the complementary signal pulses. The simulated results showed that the modulating operating frequency, carrier frequency, pure sinewave output voltage, load current, output power, and total harmonic distortions of the proposed system have 50 Hz, *1. 5 kHz*, 305.7V, 10.63A, 3250W and 0.2717% on resistive loads, and 297.8V and 10.92A, 3250W and 0.2807% on resistive-inductive loads. Sequel to the laboratory experimentation based on Table 1, the

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implemented pure sinewave, output voltage, load current, output power of 260Vpeak, 11.2A, and 2912W results under R-L Loads, indicated closely related performance characteristics between the simulated and experimented results of the proposed systems. This research work can be applied to driving low power AC motors, and its amplified version can be utilized at the receiving end of HVDC power transmission.

Further research on this work will be geared towards using the topology in higher power-level inverters.

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